MODEL 432 ANALOGUE OEM

SINGLE PHASE LOCK-IN AMPLIFIER

WITH MICRO-PROCESSOR INTERFACE

USER MANUAL V2.0

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

1 SPECIFICATIONS

Input Stage

Input Signal Modes:	Single Ended or Fully Differential, AC or DC coupled.
Input Gain:	x1, x3.3, x10, x33, x100, x330, x1000
Analogue Connections:	SMB connectors
Input Impedance:	10^{12} Ohms || 1nF, dc coupled
Maximum Inputs:	±12V DC before saturation occurs.
Gain Accuracy:	1%
Gain Stability:	200ppm/°C
Frequency:	10Hz to 100kHz

Output Stage

Output Gain:	x1, x10, x100, x1000 (Equivalent to Dynamic Reserves of 0dB, 20dB, 40dB and 80dB respectively)
Time Constant Settings:	100µs, 330µs, 1ms, 3.3ms, 10ms, 33ms, 100ms, 330ms, 1s, 3.3s, 10s, 33s
Output Offset Trim:	±1V in 256 steps

Reference Stage

Frequency:	10Hz to 100kHz
Signal Types:	Standard TTL or CMOS with mark to space ratio from 1:10 to 10:1. Rising edges only used by the instrument. Sine, triangular, square waves, etc. with amplitudes from 200mV to 10V rms.
Fine Phase Adjust:	0° to 150° in 256 steps
Coarse Phase Adjust:	0°, 90°, 180° & 270° @ reference frequency 0°, 90°, 180° & 270° @ 2 x reference frequency
Bypass:	Both the coarse and fine phase circuitry can by bypassed using jumpers.

General

Size:	100x160mm - Standard Eurocard
Digital Connector:	64 pin type C DIN41612 34 pin IDC connector
Power:	55mA @ +15V, 0V, 40mA @ -15V The device will also operate from ±12V but with reduced headroom
Computer Interface:	8 bit interface with Write signal. All settings are undefined at power up.

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2 BOARD LAYOUT

The 432 board layout is shown in Figure 1.

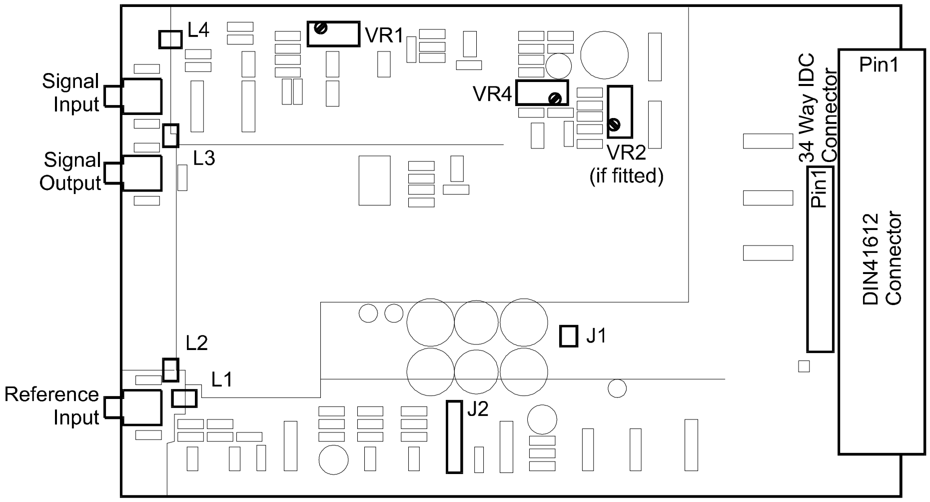

Figure 1 - 432 Board Layout

L1 - L4	Electro-Static Discharge Links
J1	Jumper that connects Analogue to Digital Gnd
J2	Allows the phase shifting circuitry to be bypassed
VR1	Signal feed through trim pot
VR2	Channel X gain adjust trim pot (may not be fitted)
VR4	Channel X offset adjust trim pot

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3 OPERATION

3.1 Basic Lock-in Amplifier Theory

Lock-in amplifiers are instruments that measure the amplitude and phase of small signals that are buried in noise. Their basic operation is that of a very narrow bandpass filter centred on the frequency of interest. This frequency is specified through the use of a reference signal input to the instrument that is of exactly the same frequency as the signal of interest. The signal is extracted through the use of a demodulator or multiplier which multiplies the input signal with the reference signal. This has the effect of frequency shifting the signal of interest to DC. The noise signals can now be removed with a simple low pass filter. The output signal will be a DC signal proportional to $A \bullet \cos(\theta)$ where A is the amplitude of the input signal and θ is the phase relationship between the input signal and the reference. As θ may be non zero, a phase shifting circuit is included in the reference circuitry to enable the maximum signal size to be found.

3.2 Full Lock-in Amplifier Theory

For lock-in amplifier theory please visit a number of pages on the Internet produced by M. Stachel of Faculty of Physics University of Konstanz Germany. It is available at http://www.lockin.de and includes theory, diagrams and a virtual Java lock-in amplifier.

3.3 Circuit Description

3.3.1 Block Diagram

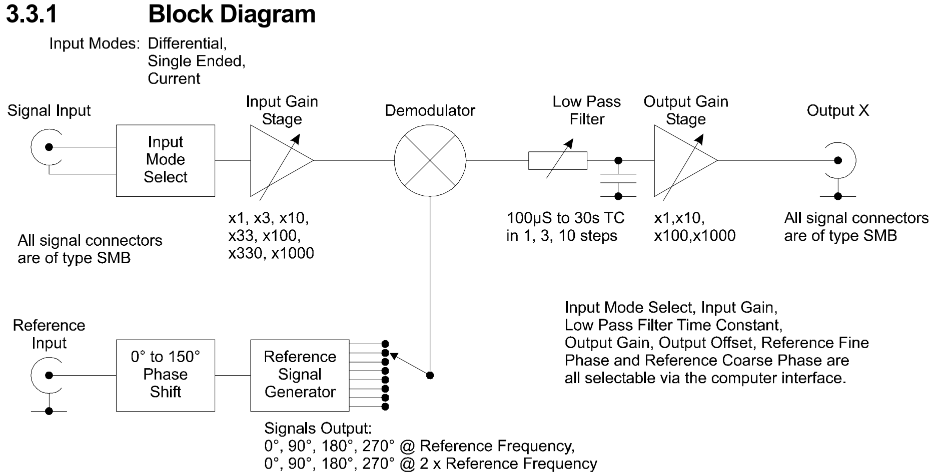

Figure 2 - 432 Block Diagram

3.3.2 Input Mode Select

To allow flexibility in the type of sensors and signal sources that the 432 is connected to, there are a number of modes that the input stage can be set up as. These include AC and DC coupling of the input, single ended or differential input and a test mode.

If a DC offset is present at the input to the demodulator, then this offset is multiplied by the reference signal producing an output square wave at the reference frequency. This signal is unwanted so it is necessary to remove all DC offset from the input signal. The 432 lock-in amplifier uses two methods for the removal of this signal. The first method is to AC couple the input. This uses a simple resistor capacitor filter and can remove up to 40V of DC offset from the input. Unfortunately, the resistor used has a high value (6M8) and this can add a significant amount of thermal noise to the input signal. It is

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therefore recommended that the input stage is DC coupled rather than AC coupled.

If the input signal is DC coupled then any DC offset is removed after the first gain stage. This has the advantage that lower resistor values can be used (470k) and the effects of thermal noise of these resistors are reduced by the gain of the first stage. The draw back is that the size of DC offset that can be removed depends on the first stage gain as follows:

Input Stage Gain	Maximum input signal + offset voltage allowed before clipping occurs when input is DC coupled
x1	±13V
x3.3	±13V
x10	±1.3V
x33	±1.3V
x100	±130mV
x330	±130mV
x1000	±130mV

It is often the case that input signals have little or no DC offset on the input signal. In these cases, simply DC couple the input stage. However, if the above limits are exceeded then the input will have to be AC coupled with the Resistor Capacitor filter.

There is often confusion as to how best to connect the signal grounds when connecting a sensor to a lock-in amplifier. The basic rule is that the ground should only be connected in one place. If the ground is connected in multiple places then earth loops can be produced which can cause noise to be inserted onto the signal being measured.

There are two main methods used: Connect the ground at the sensor or connect the ground at the lock-in. Examples of the possible connections are shown in Figure 3 and Figure 4. The choice between these two techniques is generally decided by which ever is easier to implement.

Details of the different modes and how to set the modes is shown in section 7.2.

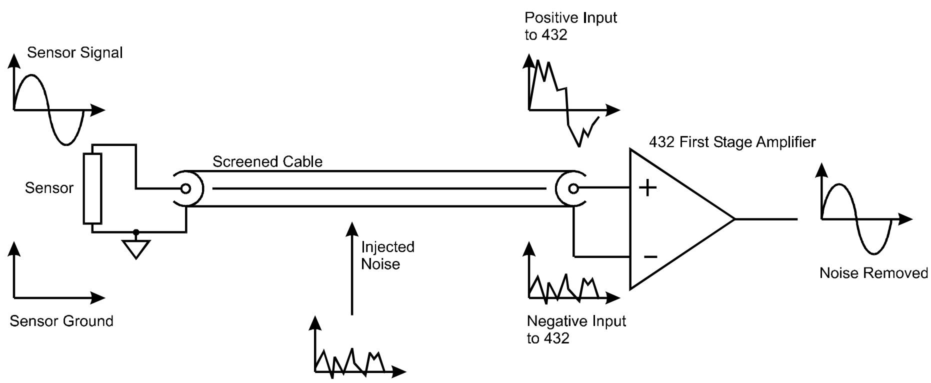

Figure 3 - Signal Ground Connected at Sensor

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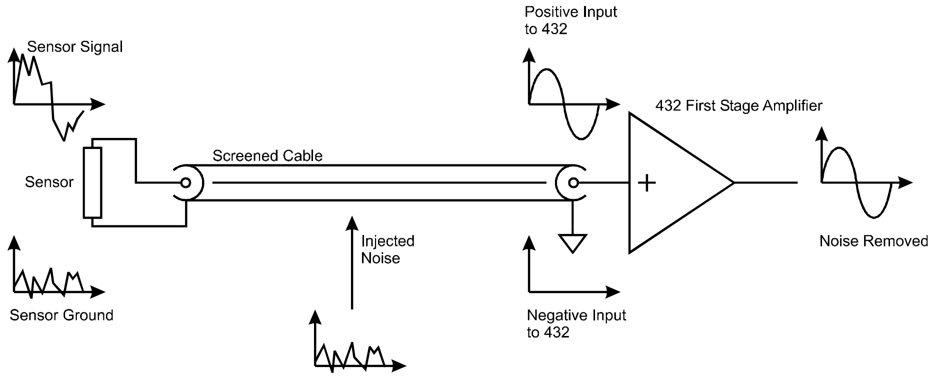

Figure 4 - Signal Ground Connected at Input to Lock-in

3.3.3 Input Stage Gain

In the 432 lock-in amplifier, there are two gain sections. One before the demodulator (Input Gain Stage) and one after the demodulator (Output Gain Stage). Both can be used to boost the input signal but it is generally best to put as much of the gain as possible in the input gain section. With low gain at the output, the offset drifts are kept to a minimum as this improves performance. Unfortunately, it also limits the dynamic reserve figure.

Full details on the input gain settings possible are given in section 7.2.

More details on gain settings and dynamic reserve are give in section 4.

3.3.4 Demodulator

The demodulator simply multiplies the input signal by either +1 or -1 dependant on the reference signal. This has the effect of shifting the signal at the reference frequency to DC. Please note that the 432 uses a square wave for demodulation which means that the signals at the third, fifth, etc harmonic of the reference signal are also converted to DC however their signal strength is attenuated by 1/3, 1/5, etc. Demodulation with a sinewave does not have this problem but suffers from greater output ripple, greater switching noise problems and is more complex.

3.3.5 Low Pass Filter

The low pass filter takes the output of the demodulator and removes the high frequency components. It is a simple first order filter with a response of that shown in Figure 5.

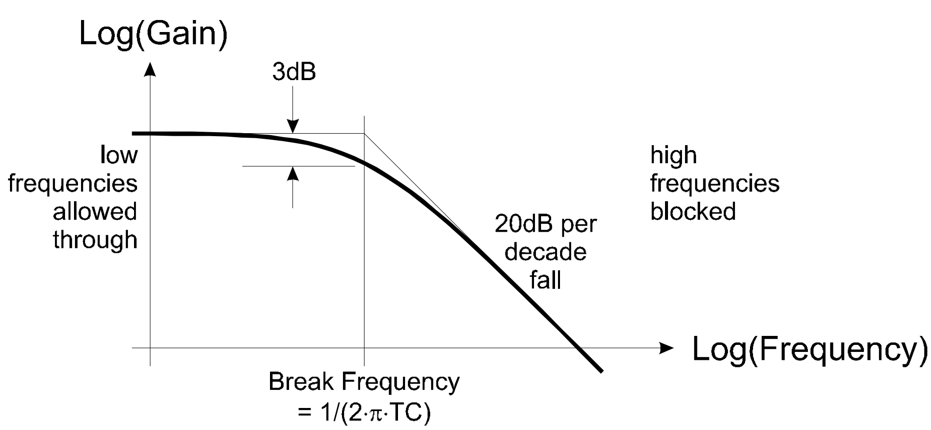

Figure 5 - Low Pass Filter Response

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Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

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The break frequency of the filter is the point at which the output is attenuated by 3dB (29%). This point is related to the Time Constant value by the equation:

Break Frequency = 1/(2•π•Time Constant)

As an example, lets consider the following:

Frequency of signal of interest - 1000Hz

Time Constant - 100mS

Hence we can calculate the break frequency:

Break Frequency = 1/(2•3.14•0.1) = 1.6Hz

This means that the low pass filter will allow through signals from DC to 1.6Hz and will attenuate signals of frequencies higher than this.

Now the demodulator will have down shifted the 1000Hz input signal to DC and hence this will pass straight through the low pass filter. However, the signals either side of the 1000Hz signal will also have been down shifted to around DC so these signals will also pass through the low pass filter with minimum attenuation.

In the above example, input signals from 998.4Hz to 1001.6Hz will be demodulated to the band DC to 1.6Hz and will pass through the low pass filter. All other signals will be attenuated.

3.3.6 Output Stage Gain

The signals at the input to the low pass filter will, in general, contain a large amount of noise. The low pass filter will reject this noise reducing the overall size of the signal. This then enables the signal to be amplified without the danger of saturation or clipping.

It is important, however, to keep the output stage gain to the minimum possible and to amplify at the input stage instead. The reason for this that the output signal of interest is at DC. This means any offset errors in the analogue circuitry after the demodulator will be mixed with signal you are trying to measure. As the size of these instrumentation offset errors are directly related to the gain in the output stage lower gains means more accurate measurements.

As an example, lets consider the following:

Input signal of interest = 10µV AC rms

Noise on input signal = ±100mV Peak

Required output signal = 1V DC

Offset error at output of demodulator = ±100µV

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Now the maximum gain we can set at the input stage is x100 as gains larger than this will cause the signal to clip.

Demodulator input signal of interest = 10μV x100 = 1mV AC rms

Demodulator input signal noise = ±100mV x 100 = ±10V Peak

The signal will then pass through the demodulator and low pass filter where the noise will be removed. However the offset error from the demodulator will be added.

Low pass filter output signal = 1mV ±100μV DC

To get the required 1V output signal now requires an output stage gain of x1000

Output from lock-in = 1mV ±100μV x1000 = 1V ±100mV DC

Fortunately, the offset error only changes slowly over time and can therefore be corrected for. This is why output offset adjustment circuitry is included on the 432 board.

More details on choosing gain settings are given in section 4.

3.3.7 Reference Circuitry

To indicate to the lock-in amplifier the frequency of the signal being measured, a reference signal is required. This signal can be sine, triangular, square wave with up to 50V DC offset or a TTL or CMOS signal. Only the rising edge of the signal is used by the reference circuitry.

The general output signal from the 432 lock-in amplifier will be a DC signal proportional to $A \bullet \cos(\theta)$ where A is the amplitude of the input signal and θ is the phase relationship between the input signal and the reference. As θ may be non zero, a phase shifting circuit is included in the reference circuitry to enable the maximum signal size to be found.

The phase shifting circuitry is split into a coarse phase adjust with 90° phase shifting steps and a fine phase adjust which covers the range 0 to 150° in 256 steps.

As the phase shifting circuitry is the limiting factor to the frequency range of operation of the instrument, both sections can be bypassed if required. This will then enable operation below 10Hz and above 100kHz. If the coarse phase shift is bypassed, it is important that the input reference signal has an exact 1:1 mark to space ratio as any discrepancy will cause errors at the output.

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United Kingdom

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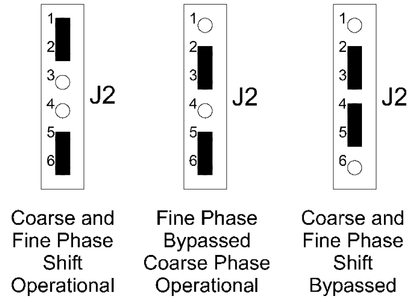

Figure 6 - Coarse and Fine Phase Shift Bypass Options

Details on how to set the different fine and coarse phase settings are given in section 7.1 & 7.4.

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4 OVERALL SYSTEM GAIN AND DYNAMIC RESERVE

To get the best performance out of the lock-in amplifier card, it is important that the gain settings at the input and at the output are correctly balanced to give optimum performance.

A high gain at the input and a low gain at the output improves noise performance and offset drift. A low gain at the input and a high gain at the output gives a high dynamic reserve at the cost of noise and offset performance.

The first stage in achieving optimum performance is to understand the features of the input signal fed into the lock-in. The different sections are shown in Figure 7.

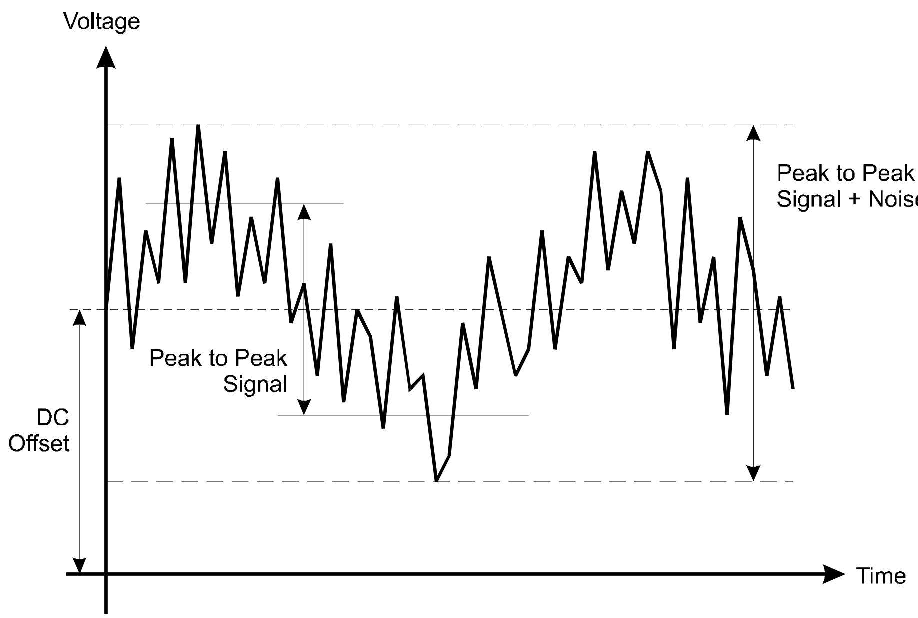

Figure 7 - Input Signal

The input wave form is generally made up from 3 components. They are:

- A sine wave (or similar) at the reference frequency
- Noise at either higher or low frequencies (or both)
- A DC offset

If the DC offset is within the limits specified in Section 3.3.2 then it can be ignored. If it is greater than this then it is necessary to AC couple the input, to remove the offset as specified in Section 7.2.

4.1 Dynamic Reserve

The dynamic reserve of the system is defined as the ratio of the noise to signal that is allowed within the system before saturation occurs, specified in dBs.

A dynamic reserve of 20dB means that the noise can be a factor of 10 larger than the signal before saturation occurs.

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A dynamic reserve of 40dB means that the noise can be a factor of 100 larger than the signal before saturation occurs.

A dynamic reserve of 60dB means that the signal can be a factor of 1000 larger than the signal before saturation occurs.

A dynamic reserve of 80dB means that the signal can be a factor of 10000 larger than the signal before saturation occurs.

Normally the signal and noise values used to calculate dynamic reserve are RMS measurements. The following explanation will use the Peak to Peak values as this is easier to understand and works for all types of noise not just white noise.

4.2 Maximum Signal Size Up To The Low Pass Filter

Assuming that the lock-in amplifier board is operating from ±15V, the maximum Peak to Peak Signal + Noise amplitude allowed before saturation occurs is 26V. The applies at all stages up to the input to the Low Pass Filter.

For example, if the input signal fed into the board has a Peak to Peak Signal + Noise value of 100mV, then the maximum gain possible at the inputs stage is 260. If a higher gain than this is required, then it is necessary to include this additional gain at the output stage. A table of gains and maximum input signal allowed is given below:

Total Input Stage Gain	Maximum Peak to Peak Signal + Noise Input Allowed Before Saturation Occurs
x 1	26V
x 3.33	7.8V
x 10	2.6V
x 33.3	780mV
x 100	260mV
x 333	78mV

Please note that the maximum gain at the input is not dependant on the amplitude of the signal you are trying to measure. The maximum gain at the input is only dependant on the amplitude of the signal + noise.

4.3 Maximum Signal Size From Low Pass Filter to Output

Once the demodulated signal has passed through the low pass filter, the noise on the signal will be reduced. This reduces the Peak to Peak Signal + Noise amplitude and allows further gain to be included in the output stage. The maximum size of gain at the output depends on the amplitude and bandwidth of the noise and also on the time constant of the low pass filter. Generally, a larger time constant will reduce the noise more allowing a greater output gain to be used.

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4.4 Example Gain Settings

The following is a list of example settings for various input signal and noise levels. This is not an exhaustive list.

Input Signal Level		Input Noise	Input Noise + Signal	Maximum Input Gain Setting	Actual Input Gain Setting	Output Gain Setting	Total System Gain	Output Voltage
RMS	P to P	P to P	P to P					DC
1 V	2.82 V	0 V	2.82 V	x 9.21	x 1	x 1	x 1	1 V
1 V	2.82 V	0 V	2.82 V	x 9.21	x 3.33	x 1	x 3.33	3.33 V
1 V	2.82 V	0 V	2.82 V	x 9.21	x 1	x 10	x 10	10 V
1 V	2.82 V	20 V	22.82 V	x 1.14	x 1	x 1	x 1	1 V
1 V	2.82 V	4 V	6.82 V	x 3.81	x 3.33	x 1	x 3.33	3.33 V
1 V	2.82 V	20 V	22.82 V	x 1.14	x 1	x 10	x 10	10 V
300 mV	848 mV	0 V	848 mV	x 30.6	x 1	x 1	x 1	300 mV
300 mV	848 mV	0 V	848 mV	x 30.6	x 3.33	x 1	x 3.33	1 V
300 mV	848 mV	0 V	848 mV	x 30.6	x 10	x 1	x 10	3 V
300 mV	848 mV	0 V	848 mV	x 30.6	x 3.33	x 10	x 33.3	10 V
300 mV	848 mV	20 V	20.9 V	x 1.24	x 1	x 1	x 1	300 mV
300 mV	848 mV	6 V	6.85 V	x 3.80	x 3.33	x 1	x 3.33	1 V
300 mV	848 mV	2 V	2.85 V	x 9.12	x 10	x 1	x 10	3 V
300 mV	848 mV	6 V	6.85 V	x 3.80	x 3.33	x 10	x 33.3	10 V
100 mV	282 mV	0 V	282 mV	x 92.2	x 1	x 1	x 1	100 mV
100 mV	282 mV	0 V	282 mV	x 92.2	x 3.33	x 1	x 3.33	333 mV
100 mV	282 mV	0 V	282 mV	x 92.2	x 10	x 1	x 10	1 V
100 mV	282 mV	0 V	282 mV	x 92.2	x 33.3	x 1	x 33.3	3.33 V
100 mV	282 mV	0 V	282 mV	x 92.2	x 10	x 10	x 100	10 V
100 mV	282 mV	20 V	20.3 V	x 1.28	x 1	x 1	x 1	100 mV
100 mV	282 mV	7 V	7.28 V	x 3.56	x 3.33	x 1	x 3.33	333 mV
100 mV	282 mV	2 V	2.28 V	x 11.4	x 10	x 1	x 10	1 V
100 mV	282 mV	400 mV	682 mV	x 38.1	x 33.3	x 1	x 33.3	3.33 V
30 mV	84.8 mV	0V	84.8 mV	x 306	x 1	x 1	x 1	30 mV
30 mV	84.8 mV	0V	84.8 mV	x 306	x 3.33	x 1	x 3.33	100 mV
30 mV	84.8 mV	0V	84.8 mV	x 306	x 10	x 1	x 10	300 mV
30 mV	84.8 mV	0V	84.8 mV	x 306	x 33.3	x 1	x 33.3	1 V
30 mV	84.8 mV	0V	84.8 mV	x 306	x 100	x 1	x 100	3 V
30 mV	84.8 mV	0V	84.8 mV	x 306	x 33.3	x 10	x 333	10 V
30 mV	84.8 mV	0V	84.8 mV	x 306	x 3.33	x 100	x 333	10 V
30 mV	84.8 mV	20V	20V	x 1.3	x 1	x 1	x 1	30 mV
30 mV	84.8 mV	7V	7.08 V	x 3.67	x 3.33	x 1	x 3.33	100 mV
30 mV	84.8 mV	2V	2.08 V	x 12.5	x 10	x 1	x 10	300 mV
30 mV	84.8 mV	600 mV	685 mV	x 38.0	x 33.3	x 1	x 33.3	1 V
30 mV	84.8 mV	100 mV	185 mV	x 141	x 100	x 1	x 100	3 V
30 mV	84.8 mV	600 mV	84.8 mV	x 38.0	x 33.3	x 10	x 333	10 V
30 mV	84.8 mV	7 V	7.08 V	x 3.67	x 3.33	x 100	x 333	10 V
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 1	x 1	x 1	10 mV
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 3.33	x 1	x 3.33	33.3 mV
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 10	x 1	x 10	100 mV
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 33.3	x 1	x 33.3	333 mV
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 100	x 1	x 100	1 V
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 333	x 1	x 333	3.33 V
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 100	x 10	x 1000	10 V
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 10	x 100	x 1000	10 V
10 mV	28.2 mV	0 V	28.2 mV	x 922	x 1	x 1000	x 1000	10 V
10 mV	28.2 mV	20 V	20 V	x 1.3	x 1	x 1	x 1	10 mV
10 mV	28.2 mV	7 V	7.02 V	x 3.7	x 3.33	x 1	x 3.33	33.3 mV
10 mV	28.2 mV	2 V	2.02V	x 12.9	x 10	x 1	x 10	100 mV
10 mV	28.2 mV	700 mV	728 mV	x 35.7	x 33.3	x 1	x 33.3	333 mV
10 mV	28.2 mV	200 mV	228 mV	x 114	x 100	x 1	x 100	1 V
10 mV	28.2 mV	40 mV	68.2 mV	x 381	x 333	x 1	x 333	3.33 V
10 mV	28.2 mV	200 mV	228 mV	x 114	x 100	x 10	x 1000	10 V
10 mV	28.2 mV	2 V	2.02 V	x 12.9	x 10	x 100	x 1000	10 V
10 mV	28.2 mV	20 V	20 V	x 1.3	x 1	x 1000	x 1000	10 V
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 1	x 1	x 1	3 mV
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 3.33	x 1	x 3.33	10 mV
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 10	x 1	x 10	30 mV
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 33.3	x 1	x 33.3	100 mV
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 100	x 1	x 100	300 mV
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 333	x 1	x 333	1 V
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 100	x 10	x 1000	3 V
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 333	x 10	x 3330	10 V
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 33.3	x 100	x 3330	10 V

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

Input Signal Level		Input Noise	Input Noise + Signal	Maximum Input Gain Setting	Actual Input Gain Setting	Output Gain Setting	Total System Gain	Output Voltage
RMS	P to P	P to P	P to P					DC
3 mV	8.48 mV	0 V	8.48 mV	x 3070	x 3.33	x 1000	x 3330	10 V
3 mV	8.48 mV	20 V	20 V	x 1.3	x 1	x 1	x 1	3 mV
3 mV	8.48 mV	7 V	7 V	x 3.7	x 3.33	x 1	x 3.33	10 mV
3 mV	8.48 mV	2 V	2 V	x 13	x 10	x 1	x 10	30 mV
3 mV	8.48 mV	700 mV	708 mV	x 36.7	x 33.3	x 1	x 33.3	100 mV
3 mV	8.48 mV	200 mV	208 mV	x 125	x 100	x 1	x 100	300 mV
3 mV	8.48 mV	60 mV	68.5 mV	x 380	x 333	x 1	x 333	1 V
3 mV	8.48 mV	200 mV	208 mV	x 125	x 100	x 10	x 1000	3 V
3 mV	8.48 mV	60 mV	68.5 mV	x 380	x 333	x 10	x 3330	10 V
3 mV	8.48 mV	700 mV	708 mV	x 36.7	x 33.3	x 100	x 3330	10 V
3 mV	8.48 mV	7 V	7 V	x 3.7	x 3.33	x 1000	x 3330	10 V
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 1	x 1	x 1	1 mV
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 3.33	x 1	x 3.33	3.33 mV
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 10	x 1	x 10	10 mV
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 33.3	x 1	x 33.3	33.3 mV
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 100	x 1	x 100	100 mV
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 333	x 1	x 333	333 mV
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 100	x 10	x 1000	1 V
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 333	x 10	x 3330	3.33 V
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 100	x 100	x 10000	10 V
1 mV	2.82 mV	0 V	2.82 mV	x 9220	x 10	x 1000	x 10000	10 V
1 mV	2.82 mV	20 V	20 V	x 1.3	x 1	x 1	x 1	1 mV
1 mV	2.82 mV	7 V	7 V	x 3.7	x 3.33	x 1	x 3.33	3.33 mV
1 mV	2.82 mV	2 V	2 V	x 13	x 10	x 1	x 10	10 mV
1 mV	2.82 mV	700 mV	703 mV	x 37.0	x 33.3	x 1	x 33.3	33.3 mV
1 mV	2.82 mV	200 mV	203 mV	x 128	x 100	x 1	x 100	100 mV
1 mV	2.82 mV	70 mV	72.8 mV	x 357	x 333	x 1	x 333	333 mV
1 mV	2.82 mV	200 mV	203 mV	x 128	x 100	x 10	x 1000	1 V
1 mV	2.82 mV	70 mV	72.8 mV	x 357	x 333	x 10	x 3330	3.33 V
1 mV	2.82 mV	200 mV	203 mV	x 128	x 100	x 100	x 10000	10 V
1 mV	2.82 mV	2 V	2 V	x 13	x 10	x 1000	x 10000	10 V
300 µV	848 µV	0 V	848 µV	x 30700	x 1	x 1	x 1	300 µV
300 µV	848 µV	0 V	848 µV	x 30700	x 3.33	x 1	x 3.33	1 mV
300 µV	848 µV	0 V	848 µV	x 30700	x 10	x 1	x 10	3.33 mV
300 µV	848 µV	0 V	848 µV	x 30700	x 33.3	x 1	x 33.3	10 mV
300 µV	848 µV	0 V	848 µV	x 30700	x 100	x 1	x 100	33.3 mV
300 µV	848 µV	0 V	848 µV	x 30700	x 333	x 1	x 333	100 mV
300 µV	848 µV	0 V	848 µV	x 30700	x 100	x 10	x 1000	333 mV
300 µV	848 µV	0 V	848 µV	x 30700	x 333	x 10	x 3330	1 V
300 µV	848 µV	0 V	848 µV	x 30700	x 100	x 100	x 10000	3.33 V
300 µV	848 µV	0 V	848 µV	x 30700	x 333	x 100	x 33300	10 V
300 µV	848 µV	0 V	848 µV	x 30700	x 33.3	x 1000	x 33300	10 V
300 µV	848 µV	20 V	20 V	x 1.3	x 1	x 1	x 1	300 µV
300 µV	848 µV	7 V	7 V	x 3.7	x 3.33	x 1	x 3.33	1 mV
300 µV	848 µV	2 V	2 V	x 13	x 10	x 1	x 10	3 mV
300 µV	848 µV	700 mV	700 mV	x 37.0	x 33.3	x 1	x 33.3	10 mV
300 µV	848 µV	200 mV	200 mV	x 128	x 100	x 1	x 100	30 mV
300 µV	848 µV	70 mV	70.8 mV	x 367	x 333	x 1	x 333	100 mV
300 µV	848 µV	200 mV	200 mV	x 128	x 100	x 10	x 1000	300 mV
300 µV	848 µV	70 mV	70.8 mV	x 367	x 333	x 10	x 3330	1 V
300 µV	848 µV	200 mV	200 mV	x 128	x 100	x 100	x 10000	3 V
300 µV	848 µV	70 mV	70.8 mV	x 367	x 333	x 100	x 33300	10 V
300 µV	848 µV	700 mV	700 mV	x 37.0	x 33.3	x 1000	x 33300	10 V
100 µV	282 µV	0V	282 µV	x 92200	x 1	x 1	x 1	100 µV
100 µV	282 µV	0V	282 µV	x 92200	x 3.33	x 1	x 3.33	333 µV
100 µV	282 µV	0V	282 µV	x 92200	x 10	x 1	x 10	1 mV
100 µV	282 µV	0V	282 µV	x 92200	x 33.3	x 1	x 33.3	3.33 mV
100 µV	282 µV	0V	282 µV	x 92200	x 100	x 1	x 100	10 mV
100 µV	282 µV	0V	282 µV	x 92200	x 333	x 1	x 333	33.3 mV
100 µV	282 µV	0V	282 µV	x 92200	x 100	x 10	x 1000	100 mV
100 µV	282 µV	0V	282 µV	x 92200	x 333	x 10	x 3330	333 mV
100 µV	282 µV	0V	282 µV	x 92200	x 100	x 100	x 10000	1 V
100 µV	282 µV	0V	282 µV	x 92200	x 333	x 100	x 33300	3.33 V
100 µV	282 µV	0V	282 µV	x 92200	x 100	x 1000	x 100000	10 V
100 µV	282 µV	20 V	20 V	x 1.3	x 1	x 1	x 1	100 µV
100 µV	282 µV	7 V	7 V	x 3.7	x 3.33	x 1	x 3.33	333 µV
100 µV	282 µV	2 V	2 V	x 13	x 10	x 1	x 10	1 mV
100 µV	282 µV	700 mV	700 mV	x 37.0	x 33.3	x 1	x 33.3	3.33 mV
100 µV	282 µV	200 mV	200 mV	x 128	x 100	x 1	x 100	10 mV

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

Input Signal Level		Input Noise	Input Noise + Signal	Maximum Input Gain Setting	Actual Input Gain Setting	Output Gain Setting	Total System Gain	Output Voltage
RMS	P to P	P to P	P to P					DC
100 µV	282 µV	70 mV	70.3 mV	x 370	x 333	x 1	x 333	33.3 mV
100 µV	282 µV	200 mV	200 mV	x 128	x 100	x 10	x 1000	100 mV
100 µV	282 µV	70 mV	70.3 mV	x 370	x 333	x 10	x 3330	333 mV
100 µV	282 µV	200 mV	200 mV	x 128	x 100	x 100	x 10000	1 V
100 µV	282 µV	70 mV	70.3 mV	x 370	x 333	x 100	x 33300	3.33 V
100 µV	282 µV	200 mV	200 mV	x 128	x 100	x 1000	x 100000	10 V
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 1	x 1	x 1	30 µV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 3.33	x 1	x 3.33	100 µV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 10	x 1	x 10	333 µV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 33.3	x 1	x 33.3	1 mV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 100	x 1	x 100	3.33 mV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 333	x 1	x 333	10 mV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 100	x 10	x 1000	33.3 mV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 333	x 10	x 3330	100 mV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 100	x 100	x 10000	333 mV
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 333	x 100	x 33300	1 V
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 100	x 1000	x 100000	3.33 V
30 µV	84.8 µV	0 V	84.8 µV	x 307000	x 333	x 1000	x 333000	10 V
30 µV	84.8 µV	20 V	20 V	x 1.3	x 1	x 1	x 1	30 µV
30 µV	84.8 µV	7 V	7 V	x 3.7	x 3.33	x 1	x 3.33	100 µV
30 µV	84.8 µV	2 V	2 V	x 13	x 10	x 1	x 10	300 µV
30 µV	84.8 µV	700 mV	700 mV	x 37.0	x 33.3	x 1	x 33.3	1 mV
30 µV	84.8 µV	200 mV	200 mV	x 128	x 100	x 1	x 100	3 mV
30 µV	84.8 µV	70 mV	70 mV	x 370	x 333	x 1	x 333	10 mV
30 µV	84.8 µV	200 mV	200 mV	x 128	x 100	x 10	x 1000	30 mV
30 µV	84.8 µV	70 mV	70 mV	x 370	x 333	x 10	x 3330	100 mV
30 µV	84.8 µV	200 mV	200 mV	x 128	x 100	x 100	x 10000	300 mV
30 µV	84.8 µV	70 mV	70 mV	x 370	x 333	x 100	x 33300	1 V
30 µV	84.8 µV	200 mV	200 mV	x 128	x 100	x 1000	x 100000	3 V
30 µV	84.8 µV	70 mV	70 mV	x 370	x 333	x 1000	x 333000	10 V
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 1	x 1	x 1	10 µV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 3.33	x 1	x 3.33	33.3 µV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 10	x 1	x 10	100 µV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 33.3	x 1	x 33.3	333 µV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 100	x 1	x 100	1 mV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 333	x 1	x 333	3.33 mV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 100	x 10	x 1000	10 mV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 333	x 10	x 3330	33.3 mV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 100	x 100	x 10000	100 mV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 333	x 100	x 33300	333 mV
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 100	x 1000	x 100000	1 V
10 µV	28.2 µV	0 V	28.2 µV	x 922000	x 333	x 1000	x 333000	3.33 V
10 µV	28.2 µV	20 V	20 V	x 1.3	x 1	x 1	x 1	10 µV
10 µV	28.2 µV	7 V	7 V	x 3.7	x 3.33	x 1	x 3.33	33.3 µV
10 µV	28.2 µV	2 V	2 V	x 13	x 10	x 1	x 10	100 µV
10 µV	28.2 µV	700 mV	700 mV	x 37.0	x 33.3	x 1	x 33.3	333 µV
10 µV	28.2 µV	200 mV	200 mV	x 128	x 100	x 1	x 100	1 mV
10 µV	28.2 µV	70 mV	70 mV	x 370	x 333	x 1	x 333	3.33 mV
10 µV	28.2 µV	200 mV	200 mV	x 128	x 100	x 10	x 1000	10 mV
10 µV	28.2 µV	70 mV	70 mV	x 370	x 333	x 10	x 3330	33.3 mV
10 µV	28.2 µV	200 mV	200 mV	x 128	x 100	x 100	x 10000	100 mV
10 µV	28.2 µV	70 mV	70 mV	x 370	x 333	x 100	x 33300	333 mV
10 µV	28.2 µV	200 mV	200 mV	x 128	x 100	x 1000	x 100000	1 V
10 µV	28.2 µV	70 mV	70 mV	x 370	x 333	x 1000	x 333000	3.33 V
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 1	x 1	x 1	3 µV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 3.33	x 1	x 3.33	10 µV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 10	x 1	x 10	30 µV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 33.3	x 1	x 33.3	100 µV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 100	x 1	x 100	300 µV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 333	x 1	x 333	1 mV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 100	x 10	x 1000	3 mV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 333	x 10	x 3330	10 mV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 100	x 100	x 10000	30 mV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 333	x 100	x 33300	100 mV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 100	x 1000	x 100000	300 mV
3 µV	8.48 µV	0 V	8.48 µV	x 3070000	x 333	x 1000	x 333000	1 V
3 µV	8.48 µV	20 V	20 V	x 1.3	x 1	x 1	x 1	3 µV
3 µV	8.48 µV	7 V	7 V	x 3.7	x 3.33	x 1	x 3.33	10 µV
3 µV	8.48 µV	2 V	2 V	x 13	x 10	x 1	x 10	30 µV

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

Input Signal Level		Input Noise	Input Noise + Signal	Maximum Input Gain Setting	Actual Input Gain Setting	Output Gain Setting	Total System Gain	Output Voltage
RMS	P to P	P to P	P to P					DC
3 µV	8.48 µV	700 mV	700 mV	x 37.0	x 33.3	x 1	x 33.3	100 µV
3 µV	8.48 µV	200 mV	200 mV	x 128	x 100	x 1	x 100	300 µV
3 µV	8.48 µV	70 mV	70 mV	x 370	x 333	x 1	x 333	1 mV
3 µV	8.48 µV	200 mV	200 mV	x 128	x 100	x 10	x 1000	3 mV
3 µV	8.48 µV	70 mV	70 mV	x 370	x 333	x 10	x 3330	10 mV
3 µV	8.48 µV	200 mV	200 mV	x 128	x 100	x 100	x 10000	30 mV
3 µV	8.48 µV	70 mV	70 mV	x 370	x 333	x 100	x 33300	100 mV
3 µV	8.48 µV	200 mV	200 mV	x 128	x 100	x 1000	x 100000	300 mV
3 µV	8.48 µV	70 mV	70 mV	x 370	x 333	x 1000	x 333000	1 V

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

5 CONNECTIONS

The external connections to the 432 lock-in amplifier are shown in Figure 8.

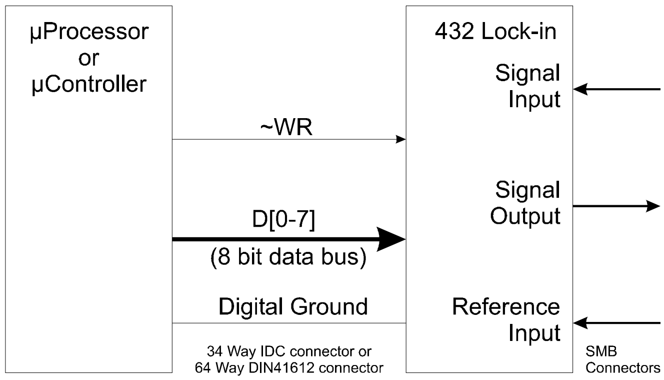

Figure 8 - External Connections

The digital connections to the µProcessor or µController are made by one of two connectors, a 34 way IDC connector or a DIN41612 connector. One or other or both of these connectors may be fitted to the 432 board.

5.1 DIN41612 Connector

The DIN41612 connector uses the following pins:

Name	Number	Description
~WR	20C	Active low WRite lines. This pin must be taken low to write data to the board. The data is latched on the rising edge of ~WR and the data should be valid 20nS before and 10nS after this edge.
D0 D1 D2 D3 D4 D5 D6 D7	3A 3C 4A 4C 5A 5C 6A 6C	Data Bus
+15V	30C	Power Connection - 55mA
0V	1A, 1C, 7C, 19C, 21C, 26A, 32A, 32C	Digital Ground Connection
-15V	30A	Power Connection - 40mA

Please note that the pin numbers are labelled on the back of the connector next to the solder pins and as per Figure 9. Please also note that some connectors have P1~A on the front face. Rather confusingly, this A is actually next to row C pins.

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

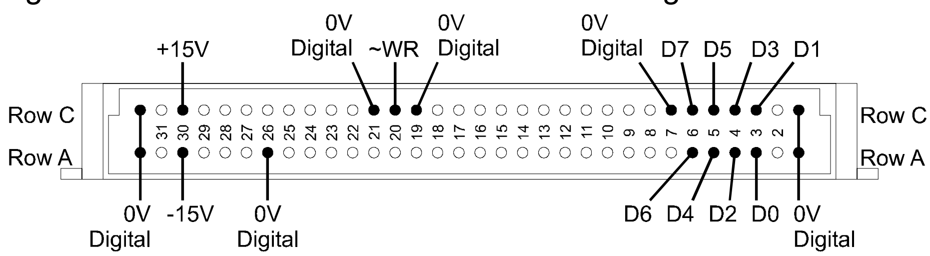

Figure 9 - 64 Pin DIN41612 Connector

5.2 34 Way IDC Connector

The 34 way IDC connector uses the following pins:

Name	Number	Description
~WR	1	Connected to Pin 23
Reserved	2	0V or unconnected
D0	3	Data Line
DGND	4	Digital Ground
D1	5	Data Bus
DGND	6	Digital Ground
D2	7	Data Line
DGND	8	Digital Ground
D3	9	Data Line
DGND	10	Digital Ground
D4	11	Data Line
DGND	12	Digital Ground
D5	13	Data Line
DGND	14	Digital Ground
D6	15	Data Line
DGND	16	Digital Ground
D7	17	Data Line
DGND	18	Digital Ground
Reserved	19	Do not connect
DGND	20	Digital Ground
Reserved	21	Do not connect
DGND	22	Digital Ground
~WR	23	Active low WRite line. This pin must taken low to write data to the board. The data is latched on the rising edge of ~WR and the data should be valid 20nS before and 10nS after this edge.
DGND	24	Digital Ground
~CS	25	Active low Chip Select line. This pin must be held low when writing data to the board.
DGND	26	Digital Ground
Reserved	27	Do not connect
Reserved	28	Do not connect
Output	29	Analogue Output from the board.
AGND	30	Ground Connection
+15V	31	Power Connection
-15V	32	Power Connection
+15V	33	Power Connection
-15V	34	Power Connection

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Pin 1 of the connector has a small triangle moulded into the plastic close to the pin. This is often difficult to find. See also Figure 10.

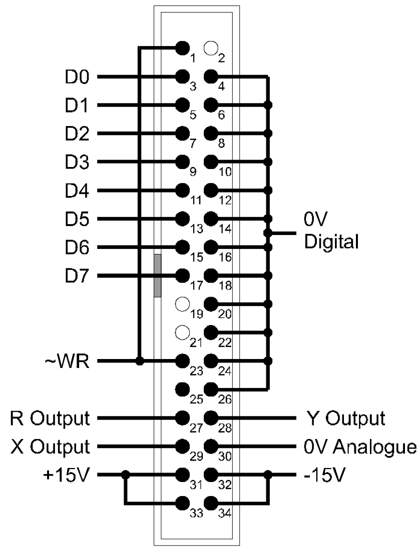

Figure 10 - 34 Way IDC Connector

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

6 POWER SUPPLY

6.1 Power Connections

A well regulated ±15V DC supply is required to power the lock-in amplifier board. Power supply filters are used onboard to drive the analogue circuitry, however the better the power supply the better the performance of the board. A ±12V DC supply can also be used to power the board but this will reduce the maximum signal size by a similar margin. E.g. A 10V rms AC input signal will be clipped as it has a peak amplitude of 14V.

6.2 Earth Connections for High Voltage / ESD Protection

As lock-in amplifiers are often used in optics applications with lasers driven by high voltage power supplies, it is sometimes important to protect equipment from high voltage discharges. Electro-Static Discharge (ESD) protection is also important and is a requirement for CE marking. All analogue inputs and outputs to the 432 are protected by transient suppression devices but for full protection a case earth connection is required directly to the PCB.

To give full protection to the board from high voltages, a thick earth wire should be bonded to the board at one or other or both of the solder pads shown in Figure 11 and connected to case or chassis ground by as short a lead as possible. If this is done then links 2 and 3 should be made and links 1 and 4 should be open circuit.

If the solder pads are not connected to case ground via a thick earth wire then links 1, 3 & 4 should be made and link 2 should be open circuit. In this case electro-static discharges will be conducted to either analogue or digital ground. As these routes pass close to sensitive components this method should be avoided if possible.

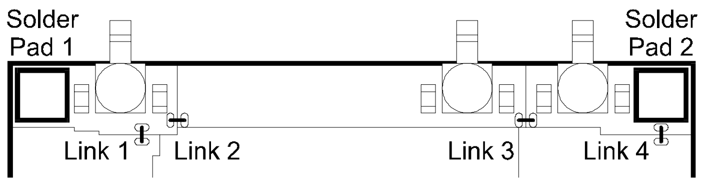

Figure 11 - Case Earth Connections

6.3 Analogue and Digital Ground

The 432 board has separate analogue and digital grounds. These grounds can be linked together on the board via a jumper (J1) or connected externally. There should not be more then 0.5V difference between the analogue and digital grounds.

Please see Figure 12 for more details.

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
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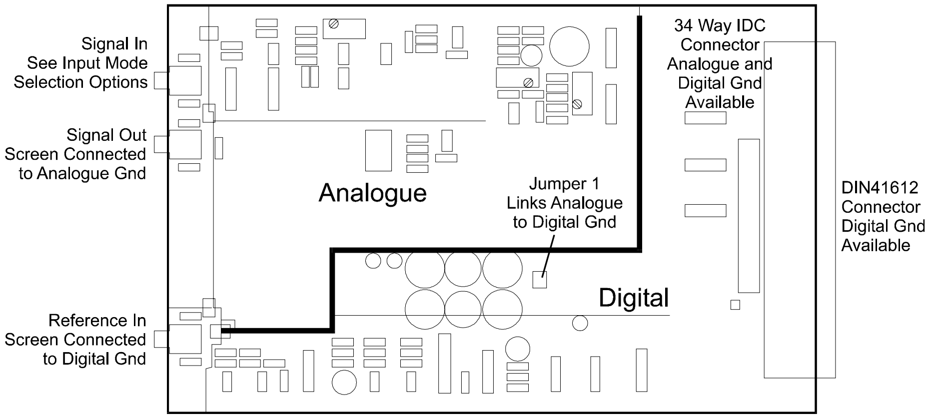

Figure 12 - Analogue and Digital Ground Connections

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North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

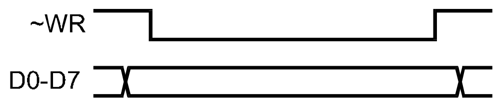
Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

7 WRITING CONTROL DATA TO THE BOARD

Data is written to the board using the ~WR and Data lines as shown below.



Data is latched on the rising edge of ~WR

A Sample Write Cycle

The data lines D5 to D7 operate effectively as address lines, selecting which signals are updated using pins D0 to D2 as shown in the following table. D3 and D4 are not used.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	-	-	PotLoadX	PotDataX	PotClk
0	0	1	-	-	-	InputMode1	InputMode0
0	1	0	-	-	InputGndPos	InputGainA1	InputGainA0
0	1	1	-	-	InputGndNeg	InputGainB1	InputGainB0
1	0	0	-	-	TimeConstantX2	TimeConstantX1	TimeConstantX0
1	0	1	-	-	-	TimeConstantX4	TimeConstantX3
1	1	0	-	-	OutputGainX2	OutputGainX1	OutputGainX0
1	1	1	-	-	ReferenceX2	ReferenceX1	ReferenceX0

As an example, to set InputGndPos to 1, InputGainA1 to 0 and InputGainA0 to 1 then the number 01000101b, 45h or 69d[*] should be written to the board.

At power up, all the above signals are in an unknown state. It therefore takes a total of eight writes to the board, one write for each of the above rows, to put the board into a known state. However, this is not enough to completely set up the board as the fine phase control and output offset circuitry requires multiple writes to PotLoadX, PotDataX and PotClk to program them.

7.1 Setting Fine Phase and Output Offset

The fine phase and output offsets are controlled with digital potentiometers. These pots are controlled by the signals PotLoadX, PotDataX and PotClk which operates as a serial interface.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	-	-	PotLoadX	PotDataX	PotClk

At power up, PotLoadX, PotDataX and PotClk are in an unknown state. After power up these signals should all be set to 0. This is achieved by writing 00000000b, 00h or 0d to the board.

[*] 01000101b means the number 01000101 in binary, 45h means the number 45 in hex and 69d means the number 69 in decimal.

Bartles Industrial Estate
North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

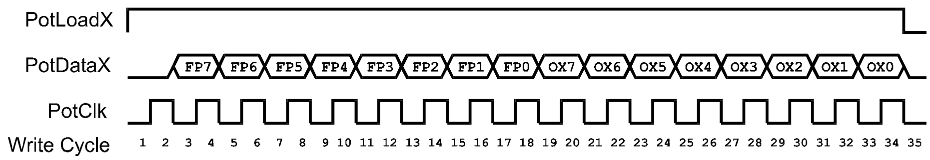
i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

To set the values of the fine phase and output offset, a total of 35 writes need to be made to the board, with the data being output serially to PotDataX. The actual data is loaded on the 35th write cycle. This process is shown below.



Writing Data to the Digital Potentiometers

The values FP7 to FP0 combine to produce an 8 bit number which controls the Fine Phase setting. Example values are shown below.

FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	Binary	Hex	Decimal	Fine Phase Shift Setting
0	0	0	0	0	0	0	0	00000000	00	0	0°
0	0	0	0	0	0	0	1	00000001	01	1	0.59°
0	1	0	0	1	1	0	1	01001101	4D	77	45.29°
1	0	0	0	0	0	0	0	10000000	80	128	75.29°
1	0	0	1	1	0	0	1	10011001	99	153	90°
1	1	1	1	1	1	1	1	11111111	FF	255	150°

The values of OX7 to OX0 combine to produce an 8 bit number which controls the X channel output offset. Example values are shown below.

OX7	OX6	OX5	OX4	OX3	OX2	OX1	OX0	Binary	Hex	Decimal	Output Offset Setting
0	0	0	0	0	0	0	0	00000000	00	0	-1V
0	0	0	0	0	0	0	1	00000001	01	1	-0.992V
0	1	0	0	0	0	0	0	01000000	40	64	-0.5V
1	0	0	0	0	0	0	0	10000000	80	128	0V
1	1	0	0	0	0	0	0	11000000	C0	192	+0.5V
1	1	1	1	1	1	1	1	11111111	FF	255	0.992V

As a final example, to set the fine phase setting to 45.3° (FP=01001101b) and to set the X channel output offset to +0.5V (OX=11000000) it is necessary to send the following 35 values to the board:

Write Cycle	Value in Binary	Value in Hex	Value in Decimal	Description
1	00000100	04	4	-
2	00000101	05	5	-
3	00000100	04	4	FP7
4	00000101	05	5	FP7
5	00000110	06	6	FP6
6	00000111	07	7	FP6
7	00000100	04	4	FP5
8	00000101	05	5	FP5
9	00000100	04	4	FP4
10	00000101	05	5	FP4
11	00000110	06	6	FP3
12	00000111	07	7	FP3
13	00000110	06	6	FP2
14	00000111	07	7	FP2
15	00000100	04	4	FP1

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North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

Write Cycle	Value in Binary	Value in Hex	Value in Decimal	Description
16	00000101	05	5	FP1
17	00000110	06	6	FP0
18	00000111	07	7	FP0
19	00000110	06	6	OX7
20	00000111	07	7	OX7
21	00000110	06	6	OX6
22	00000111	07	7	OX6
23	00000100	04	4	OX5
24	00000101	05	5	OX5
25	00000100	04	4	OX4
26	00000101	05	5	OX4
27	00000100	04	4	OX3
28	00000101	05	5	OX3
29	00000100	04	4	OX2
30	00000101	05	5	OX2
31	00000100	04	4	OX1
32	00000101	05	5	OX1
33	00000100	04	4	OX0
34	00000101	05	5	OX0
35	00000000	00	0	load

7.2 Input Stage Settings

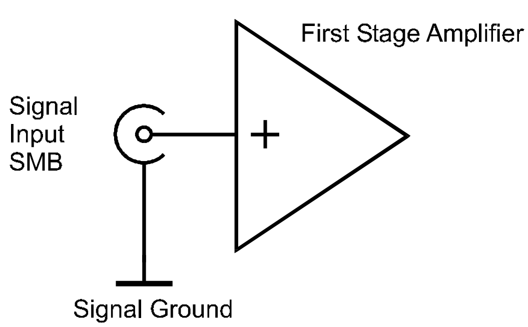
The input stage settings allow a number of different options to be used as the input to the lock-in amplifier board. The signals used to control the input stage are as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	-	-	-	InputMode1	InputMode0
0	1	0	-	-	InputGndPos	InputGainA1	InputGainA0
0	1	1	-	-	InputGndNeg	InputGainB1	InputGainB0

InputGndPos, InputGndNeg, InputMode0 & InputMode1 set the mode of operation of the input stage. InputGainA0, A1, B0 & B1 set the gain for the input stage.

There are 6 different modes of the input stage and these are set as follows:

Single Ended DC Coupled



InputMode0	0
InputMode1	1
InputGndPos	1
InputGndNeg	0

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Redruth
Cornwall TR15 1HR
United Kingdom

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f. +44 [0]1209 314609
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i. www.scitec.uk.com
e. scitec@scitec.uk.com

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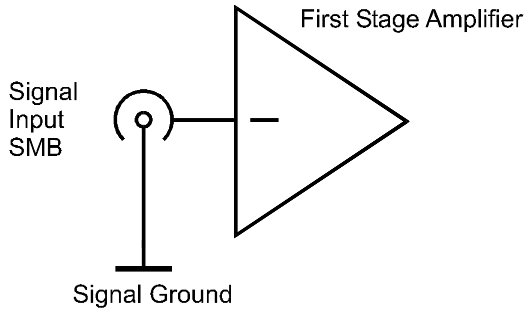
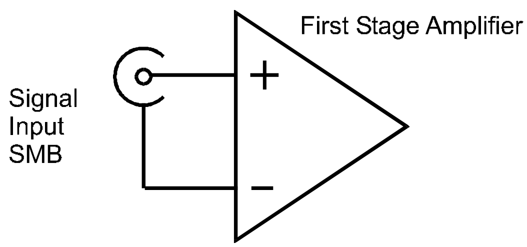
Single Ended DC Coupled Centre Ground



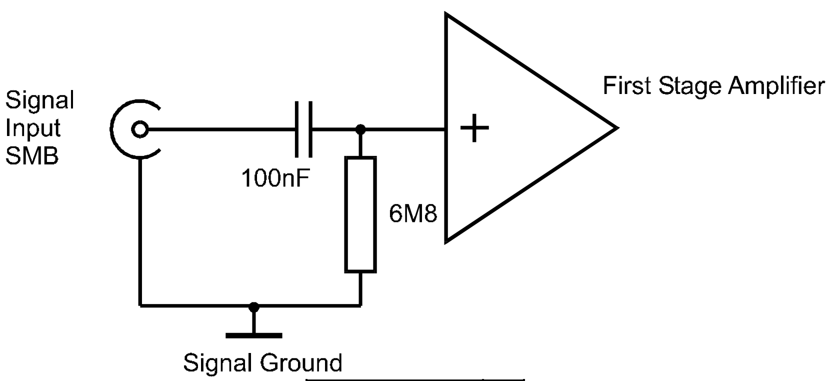
InputMode0	0
InputMode1	1
InputGndPos	0
InputGndNeg	1

Differential DC Coupled



InputMode0	0
InputMode1	1
InputGndPos	1
InputGndNeg	1

Single Ended AC Coupled



InputMode0	1
InputMode1	0
InputGndPos	1
InputGndNeg	0

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North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
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West Sussex
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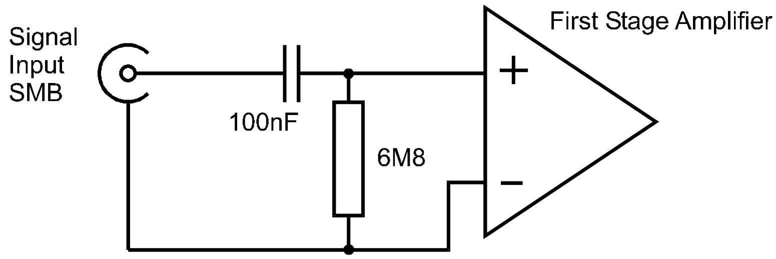
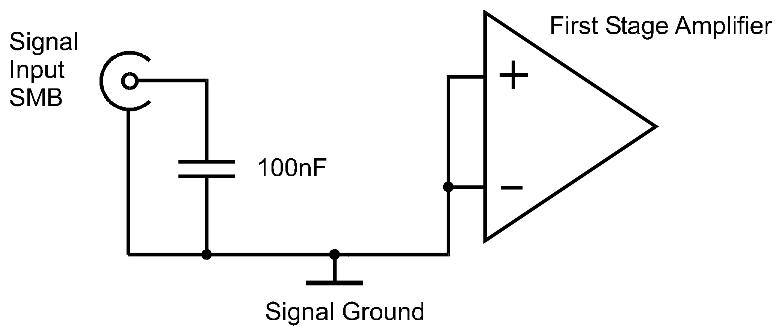
Differential AC Coupled



InputMode0	1
InputMode1	0
InputGndPos	1
InputGndNeg	1

Inputs Shorted

This mode can be useful as a test mode. Please note that the input SMB connector is shorted by a 100nF capacitor.



InputMode0	1
InputMode1	0
InputGndPos	0
InputGndNeg	0

The input gain stages are set as follows:

		Input Gain Stage A	
InputGainA1	InputGainA0	Nominal	Actual
1	1	x1	x1.00
1	0	x10	x9.90
0	1	x100	x100.2
0	0	x110	x110.1

		Input Gain Stage B	
InputGainB1	InputGainB0	Nominal	Actual
1	1	x1	x1.00
1	0	x3.33	x3.32
0	1	x10	x9.90
0	0	x12	x12.22

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North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

7.3 Output Stage Settings

The low pass filter between the demodulator and the output gain stage has its time constant set by the signals TimeConstantX0 to X4. The gain of the output stage is set by OutputGainX0 to X2.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	-	-	TimeConstantX2	TimeConstantX1	TimeConstantX0
1	0	1	-	-	-	TimeConstantX4	TimeConstantX3
1	1	0	-	-	OutputGainX2	OutputGainX1	OutputGainX0

The time constant settings possible are as follows:

TimeConstantX						
X4	X3	X2	X1	X0	Nominal	Actual
1	1	0	0	0	-	82µS
1	1	1	0	0	-	87µS
1	1	0	1	0	100µS	98µS
1	1	1	1	0	-	105µS
1	1	0	0	1	330µS	330µS
1	1	1	0	1	-	430µS
1	1	0	1	1	1mS	990µS
1	1	1	1	1	3.3mS	3.3mS
1	0	0	0	0	-	8.2mS
1	0	1	0	0	-	8.7mS
1	0	0	1	0	10mS	9.8mS
1	0	1	1	0	-	10.5mS
1	0	0	0	1	33mS	33.0mS
1	0	1	0	1	-	43.0mS
1	0	0	1	1	100mS	99mS
1	0	1	1	1	330mS	330mS
0	1	0	0	0	-	820mS
0	1	1	0	0	-	870mS
0	1	0	1	0	1S	980mS
0	1	1	1	0	-	1.05S
0	1	0	0	1	3.3S	3.30S
0	1	1	0	1	-	4.30S
0	1	0	1	1	10S	9.9S
0	1	1	1	1	33S	33S

Output Gain Settings are as follows:

			Output Gain Stage	
OutputGainX2	OutputGainX1	OutputGainX0	Nominal	Actual
1	1	1	x1	x1.00
1	1	0	x10	x11
1	0	1	x100	x101
1	0	0	-	x110
0	1	1	x1000	x1001
0	1	0	-	x1010
0	0	1	-	x1100
0	0	0	-	x1110

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North Street
Redruth
Cornwall TR15 1HR
United Kingdom

t. +44 [0]1209 314608
f. +44 [0]1209 314609
f2. +44 [0]870 1600860

i. www.scitec.uk.com
e. scitec@scitec.uk.com

Director. JW Smith Ph.D

Scitec Instruments Ltd
Registered in England
No. 1535664

Registered Office
1 Jefferson Court
6 Marine Drive West
Bognor Regis
West Sussex
PO21 2QA

7.4 Reference Settings

By changing the control signals ReferenceX0 to X2, it is possible to phase shift the reference signal in 90° increments and to double the demodulation frequency.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	-	-	ReferenceX2	ReferenceX1	ReferenceX0

ReferenceX2	ReferenceX1	ReferenceX0	Coarse Phase
0	1	0	0° @ 2 x Ref
0	1	1	90° @ 2 x Ref
0	0	0	180° @ 2 x Ref
0	0	1	270° @ 2 x Ref
1	1	0	0° @ Ref
1	1	1	90° @ Ref
1	0	0	180° @ Ref
1	0	1	270° @ Ref

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North Street
Redruth
Cornwall TR15 1HR
United Kingdom

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f. +44 [0]1209 314609
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i. www.scitec.uk.com
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